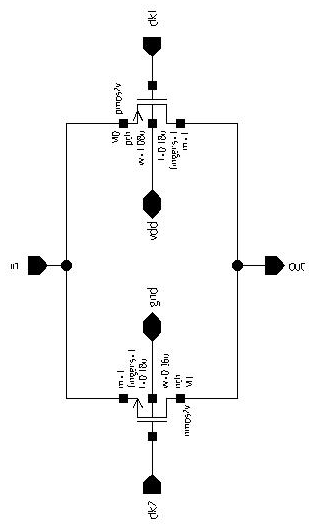
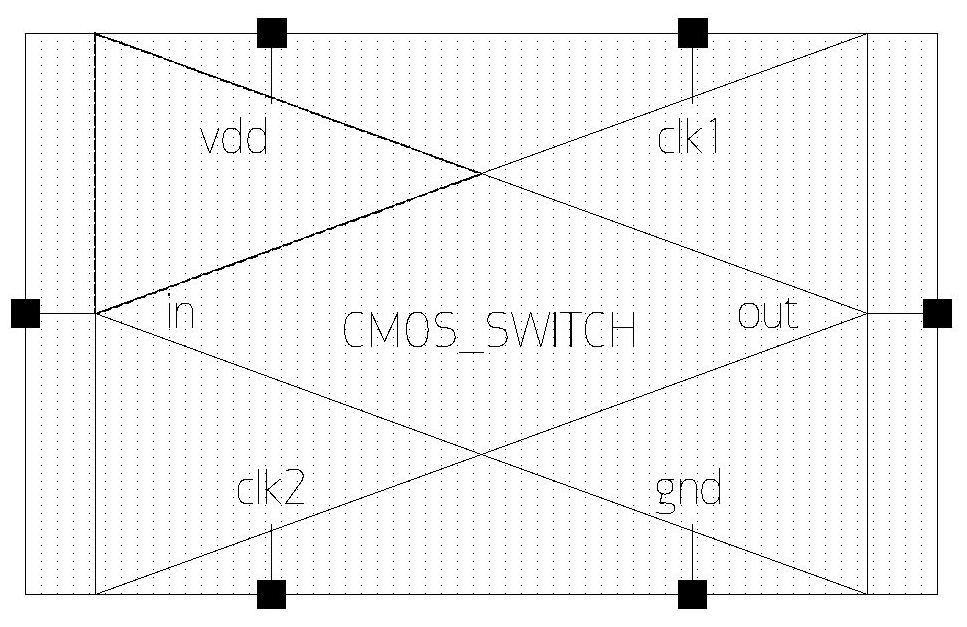
**GIL MICHAEL E. REGALADO BS ECE IV EE 272**

**LABORATORY CMOS TRANSMISSION GATE (CMOS SWITCH)**

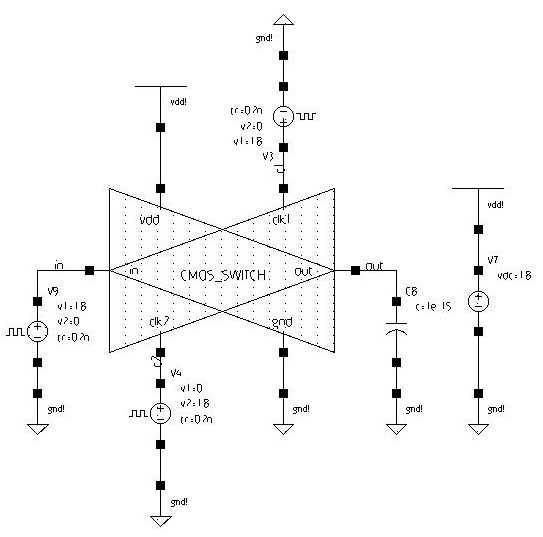
SCHEMATIC



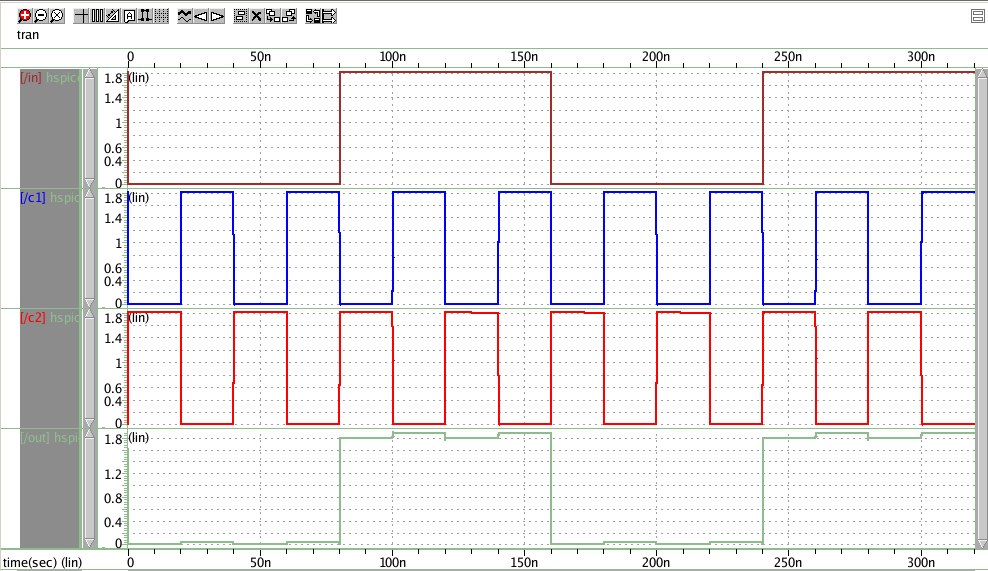
SYMBOL

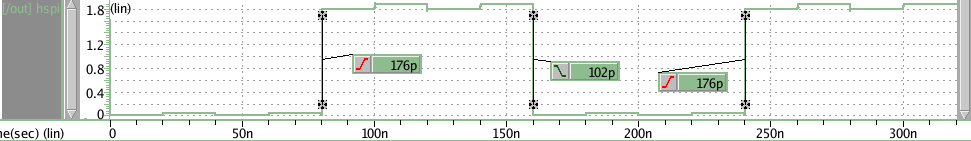


TEST BENCH



SIMULATION





The CMOS Transmission Gate is constructed by parallel connection of PMOS and NMOS transistors, with complementary gate signals. The CMOS switch works like a voltage-controlled switch, similar to an electromagnetic relay with one normally open circuit. It consists of one n-channel and one p-channel transistors with common source and drain connections.

In the circuit at the testbench clock 1 controls the PMOS (where low is switch on) and clock 2 controls NMOS (where high is switch on). When clock 1 is 0 and clock 2 is 1, the switch is close and the input signal can flow through the transmission gate, otherwise it can’t and the transmission gate acts as an open circuit.